of JFET **710** is enabled by biasing the switching device **702** transistor to conduct. In one embodiment, the switching device **702** transistor comprises a bipolar transistor. In one such embodiment, the transistor is of type PNP. In one embodiment, converter **790** and drain D of JFET **710** are coupled to a ground Gnd.

FIG. **8** depicts a switching circuit **800**, according to one embodiment of the present invention. Switching circuit **800** includes a driver device **801**. Driver device **801** has a signal input Vin, a supply voltage input Vcc, and an output, which is coupled to a capacitance C**806**. In one embodiment, driver device **801** comprises a device characteristic of those for driving MOSFETs.

Capacitance C**806** capacitively couples the output of driver device **801** to a JFET **810** having a gate G, a source S, and a drain D. A converter **890** couples to JFET **810** and provides an output Vout of switching circuit **800**. A switching device **802** couples switching circuit **800** output Vout to the gate G of JFET **810**.

Switching circuit **800** output provides voltage to drive the gate G of JFET **810** upon enabling by the signal input Vin of the driver device **801**. In one embodiment, the switching device **802** comprises a transistor (e.g., and related biasing circuitry). Coupling switching circuit **800** output voltage Vout to gate G of JFET **810** is enabled by biasing the switching device **802** transistor to conduct. In one embodiment, the switching device **802** transistor comprises a bipolar transistor. In one such embodiment, the transistor is of type PNP.

Switching circuit **800** also comprises a JFET **820**, which is coupled to JFET **810** at a phase node **899**, from drain D' of JFET **820** to source S of JFET **810**. JFETs **810** and **820** are characterized by the same mode type, and in one embodiment comprise enhancement mode JFETs. JFETs **810** and **820** respectively conduct during different phase cycles one from another. For instance, JFET **810** conducts when Vin swings negative and JFET **820** conducts when Vin swings positive. Thus, JFET **820** functions as a high side JFET and JFET **810** functions as a low side JFET for switching circuit **800**. In one embodiment, converter **890** and drain D of JFET **810** are coupled to a ground Gnd.

In one embodiment, switching circuit **800** includes a switched capacitor **850**. Switched capacitor **850** provides current to drive high side JFET **820**, such as with developing bias voltage through a resistance **857**. Switched capacitor **850** switches to drive JFET **820** when JFET **810** cuts off. When JFET **820** cuts off, the switched capacitor **850** is charged by Vout. When JFET **820** is conducting, the gate G of JFET **810** is held at a negative voltage. In one embodiment, this negative voltage is in a range substantially between −3 Volts and −10 Volts. In one embodiment, Vout is in a range substantially between 1 Volt and 3.5 Volts. In one embodiment, switching circuit **800** (or e.g., switching circuit **700**; FIG. **7**) comprises part of a direct current (DC) converter.

In summary, a switching circuit of an embodiment of the present invention includes a driver device having a signal input, a supply voltage input, and an output. The driver output is coupled (e.g., capacitively) to a JFET (e.g., an enhancement mode JFET). A converter (e.g., a DC converter) couples to the JFET and provides an output of the switching circuit. When enabled, a switching device couples this switching circuit output to the gate of the JFET, thus causing the JFET to be driven into conduction.

Embodiments of the present invention, a circuit and method for driving a field effect transistor gate, are thus described. While the present invention has been described in particular embodiments, it should be appreciated that the present invention should not be construed as limited by such embodiments, but rather construed according to the following claims and their equivalents.

What is claimed is:

1. A switching circuit comprising:

a driver device having a signal input, a supply voltage input, and an output;

a junction field effect transistor having a gate, a source, and a drain, wherein said driver device output is capacitively coupled to said gate;

a converter coupled to said junction field effect transistor and providing an output of said switching circuit; and

a switching device for receiving said switching circuit output as an input signal and providing a voltage to drive said gate, wherein said switching device is enabled with said driver device signal input.

2. The switching circuit of claim **1** wherein said switching device comprises a transistor and wherein said switching device is enabled by biasing said switching device transistor to conduct.

3. The switching circuit of claim **2** wherein said transistor comprises a bipolar transistor.

4. The switching circuit of claim **3** wherein said bipolar transistor comprises a type PNP transistor.

5. The switching circuit of claim **1** wherein said junction field effect transistor comprises an enhancement mode junction field effect transistor.

6. The switching circuit of claim **1** wherein said junction field effect transistor comprises a first junction field effect transistor, said switching circuit further comprising a second junction field effect transistor wherein said second junction field effect transistor is coupled to said first junction field effect transistor, wherein said first and said second junction field effect transistors are characterized by the same mode type, and wherein said first and said second junction field effect transistors conduct during different phase cycles one from another.

7. The switching circuit of claim **6** further comprising a switched capacitor, wherein said switched capacitor provides a current to bias a gate of said second junction field effect transistor and wherein said switched capacitor is charged with said switching circuit output.

8. The switching circuit of claim **1** wherein, when said junction field effect transistor is not conducting, said gate is held at a negative voltage.

9. The switching circuit of claim **1** wherein said driver device comprises a metal oxide semiconductor field effect transistor driver.

10. A method for driving a junction field effect transistor in a converter circuit, said method comprising:

enabling a switching mechanism to conduct;

upon said enabling, receiving an output voltage of said converter circuit as an input signal to the switching mechanism and providing a voltage to drive a gate of said junction field effect transistor; and

upon said coupling, driving said junction field effect transistor to conduct.

11. The method of claim **10** wherein said switching mechanism comprises a switching transistor and wherein said enabling comprises coupling an input signal for said converter circuit to bias said switching transistor to conduct.

12. The method of claim **11** wherein said junction field effect transistor comprises a first junction field effect transistor, said converter circuit also having a second junction field effect transistor, said second junction field effect transistor coupled to said first junction field effect transistor, and